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TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED)

INVENTOR NAME: Priyavadan R. Patel et al. SERIAL NO.: 10/006,292

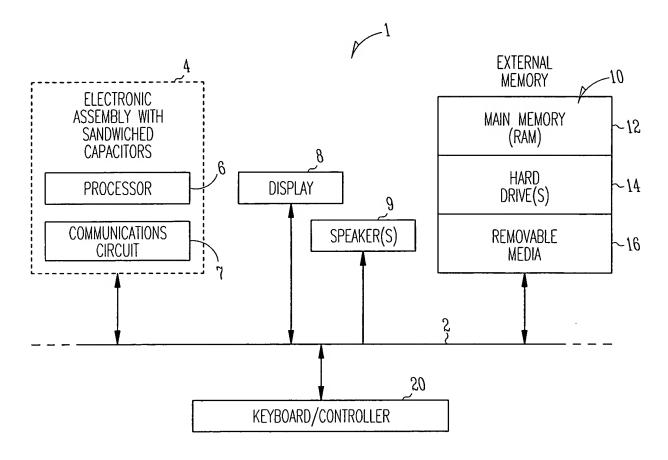


Fig. 1

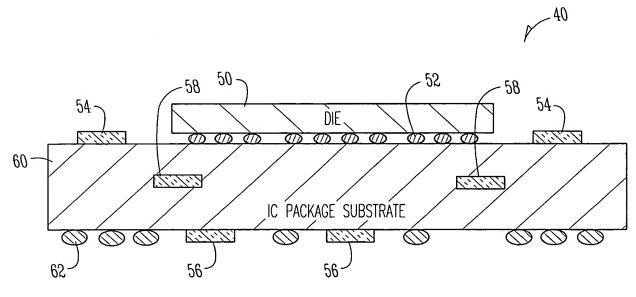


Fig.2 (Prior Art)

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED)

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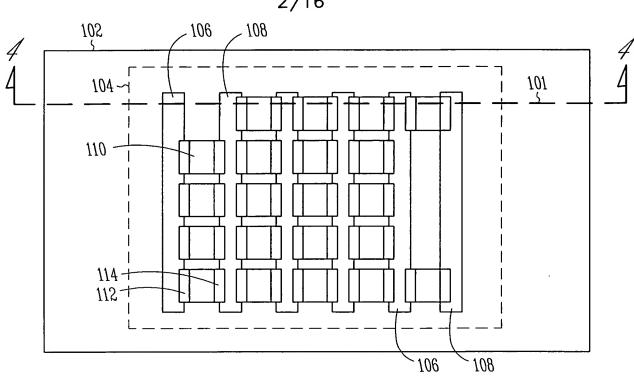


Fig. 3

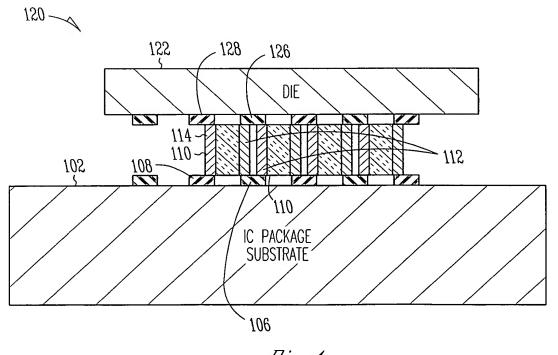


Fig. 4

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED) INVENTOR NAME: Priyavadan R. Patel et al.

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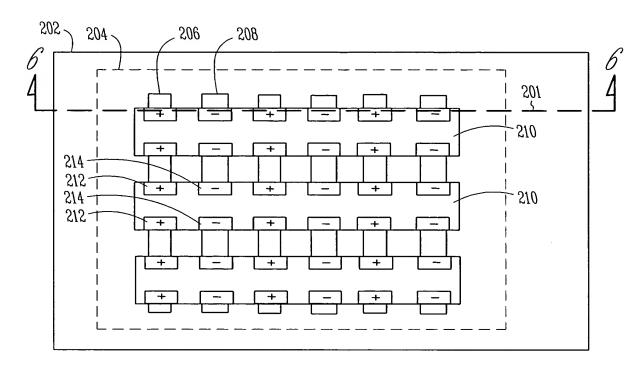
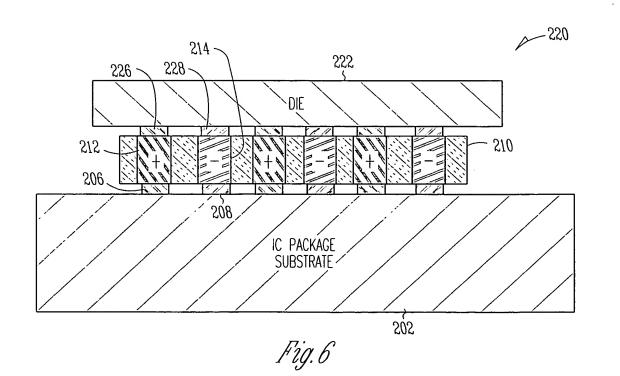
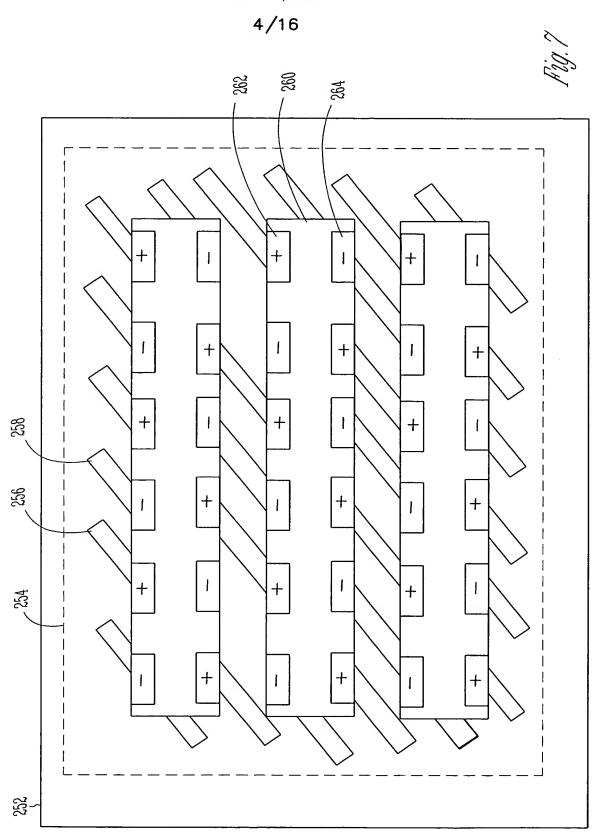


Fig. 5



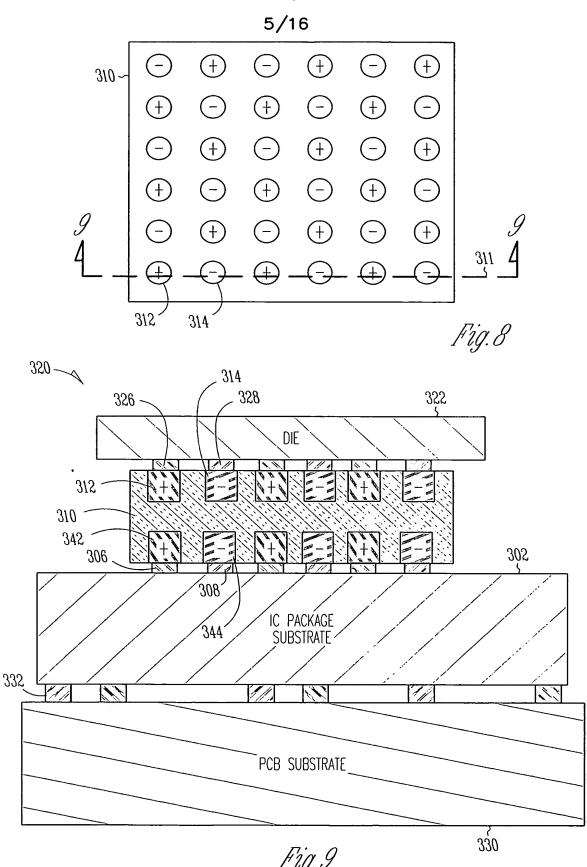
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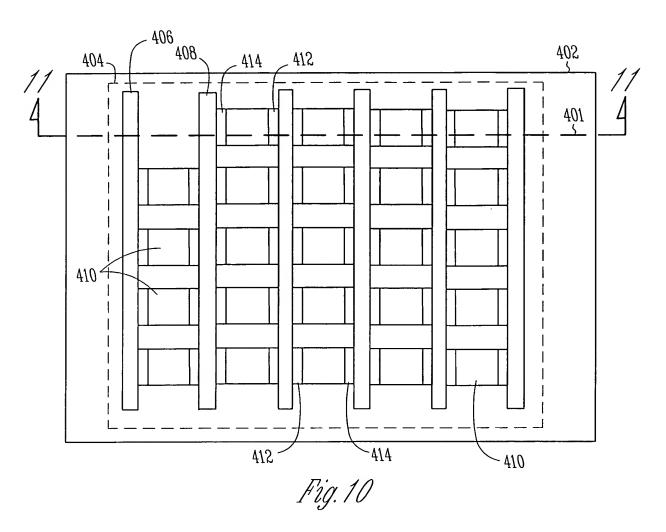


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410 420 412 414 422 DIE 426-1 428 - 416 402 408 406 -IC PACKAGE SUBSTRATE

Fig. 11

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED) INVENTOR NAME: Priyavadan R. Patel et al.

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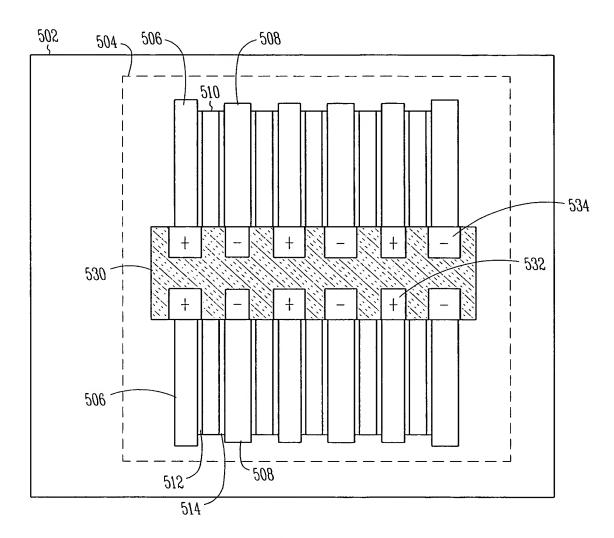
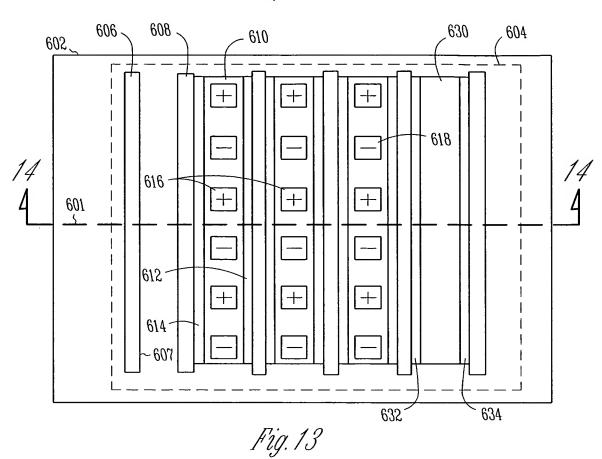
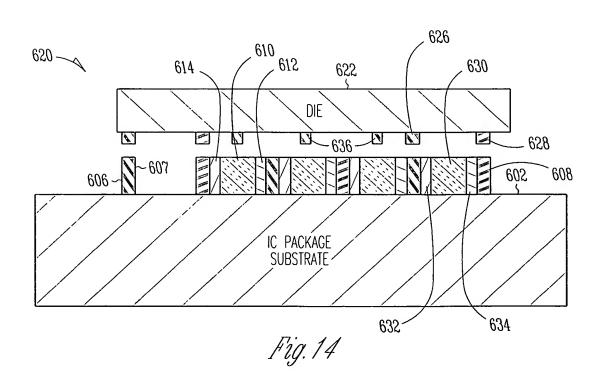


Fig. 12

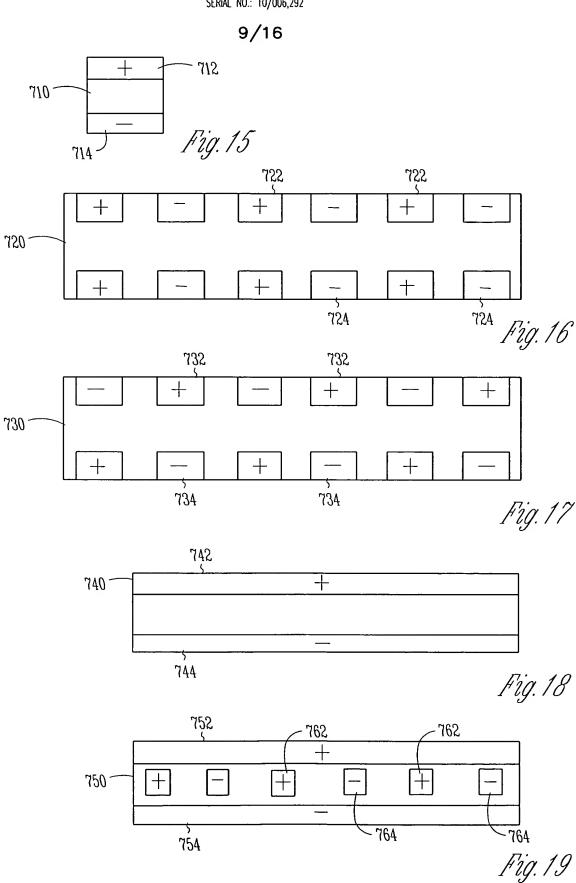
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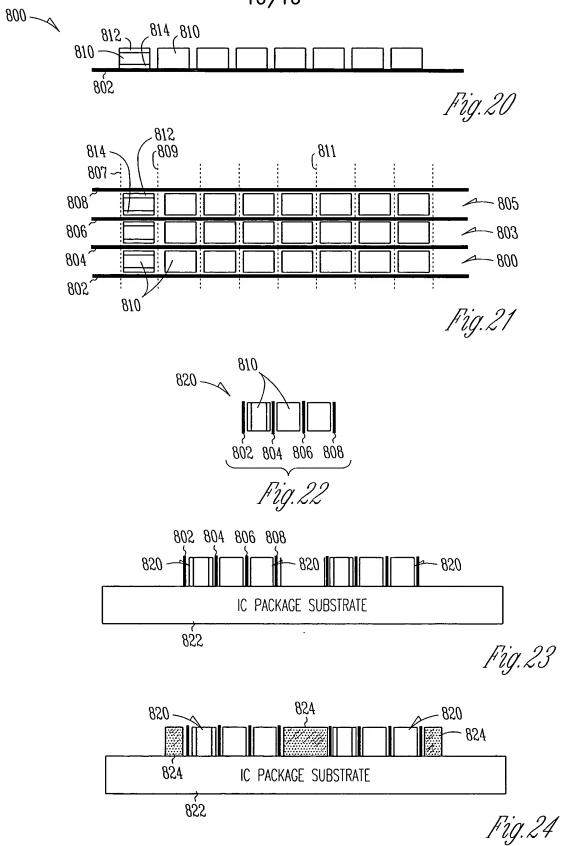


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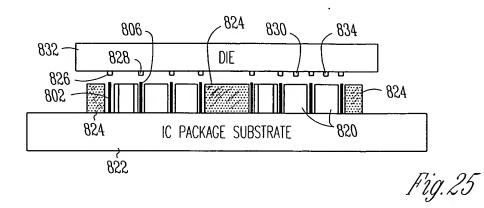


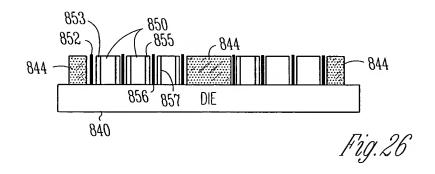
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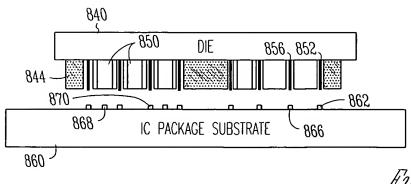
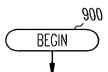


Fig.27

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED) INVENTOR NAME: Priyavadan R. Patel et ol.

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OBTAIN AND/OR MAKE CAPACITORS AND AN IC PACKAGE SUBSTRATE [FOR AN EMBODIMENT WHEREIN CAPACITORS ARE TO BE PLACED ON AN IC PACKAGE SUBSTRATE]

[FOR AN ALTERNATIVE EMBODIMENT, WHEREIN CAPACITORS ARE TO BE PLACED ON AN IC: OBTAIN OR MAKE AN IC]

- THE CAPACITORS CAN BE OF ANY TYPE, INCLUDING DISCRETE, ARRAY, INTERDIGITATED, CAPACITOR ASSEMBLIES, ETC.
- EACH CAPACITOR OR CAPACITOR ASSEMBLY HAS TERMINALS OF FIRST AND SECOND POLARITY TYPES

ARRANGE ONE OR MORE CAPACITORS AND/OR CAPACITOR ASSEMBLIES ON A SURFACE OF THE IC PACKAGE SUBSTRATE WITHIN AN IC MOUNTING REGION

[FOR ALTERNATIVE EMBODIMENT: ARRANGE THE ONE OR MORE CAPACITORS AND/OR CAPACITOR ASSEMBLIES ON A SURFACE OF THE IC]

- THE SUBSTRATE SURFACE [ALTERNATIVE EMBODIMENT: IC SURFACE] HAS A PLURALITY OF CONDUCTORS, INCLUDING A FIRST SET TO CONDUCT A FIRST POTENTIAL, AND A SECOND SET TO CONDUCT A SECOND POTENTIAL

A

Fig.28A

905

904

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED)

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A

904 CONT'D

- THE CONDUCTORS CAN BE OF ANY SUITABLE TYPE, SUCH AS SURFACE TRACES, PADS, OR BARS
- THE ONE OR MORE CAPACITORS AND/OR CAPACITOR ASSEMBLIES ARE ARRANGED SUCH THAT CERTAIN TERMINALS OF THE FIRST POLARITY TYPE CONTACT THE FIRST SET OF CONDUCTORS, AND CERTAIN TERMINALS OF THE SECOND POLARITY TYPE CONTACT THE SECOND SET OF CONDUCTORS
- IF THE IC PACKAGE SUBSTRATE SURFACE
 [ALTERNATIVE EMBODIMENT: IC SURFACE] HAS
 CONDUCTIVE BARS, ONE OR MORE OF THE
 CAPACITORS AND/OR CAPACITOR ASSEMBLIES IS
 POSITIONED BETWEEN ADJACENT ONES OF THE BARS

SECURE THE CAPACITORS AND/OR CAPACITOR
ASSEMBLIES TO THE SUBSTRATE SURFACE
[ALTERNATIVE EMBODIMENT: TO THE IC SURFACE]
USING A SUITABLE MECHANISM

 E.G., APPLY A FILL OR ADHESIVE MATERIAL TO THE CAPACITORS AND/OR CAPACITOR ASSEMBLIES, AND/OR OPENINGS BETWEEN THE CAPACITORS AND/OR CAPACITOR ASSEMBLIES; USE SPACERS OR CLAMPS; ETC.

908

906

POSITION AND MOUNT AN IC ON THE MOUNTING REGION, E.G. USING SOLDER REFLOW

 ELECTRICALLY COUPLE THE IC TERMINALS TO CORRESPONDING TERMINALS OF THE ONE OR MORE CAPACITORS AND/OR CAPACITOR ASSEMBLIES, AND OPTIONALLY TO CONDUCTORS ON THE SUBSTRATE

B)

Fig.28B

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED) INVENTOR NAME: Priyavadan R. Patel et al.

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308 CONL, D

- IF THE IC PACKAGE SUBSTRATE SURFACE HAS CONDUCTIVE BARS, ONE OR MORE OF THE CAPACITORS AND/OR CAPACITOR ASSEMBLIES CAN BE ELECTRICALLY COUPLED TO ONE OR MORE BARS, TO THE IC, OR TO ONE OR MORE BARS AND TO THE IC

[FOR ALTERNATIVE EMBODIMENT: POSITION AND MOUNT THE IC ON A MOUNTING REGION OF AN IC PACKAGE SUBSTRATE, E.G. USING SOLDER REFLOW]

- [ALTERNATIVE EMBODIMENT: ELECTRICALLY COUPLE THE IC PACKAGE SUBSTRATE TERMINALS TO CORRESPONDING TERMINALS OF THE ONE OR MORE CAPACITORS AND/OR CAPACITOR ASSEMBLIES, AND OPTIONALLY TO CONDUCTORS ON THE IC]
- [ALTERNATIVE EMBODIMENT: IF THE IC SURFACE HAS CONDUCTIVE BARS, ONE OR MORE OF THE CAPACITORS AND/OR CAPACITOR ASSEMBLIES CAN BE ELECTRICALLY COUPLED TO ONE OR MORE BARS, TO THE IC PACKAGE SUBSTRATE, OR TO ONE OR MORE BARS AND TO THE IC PACKAGE SUBSTRATE]



Fig.280

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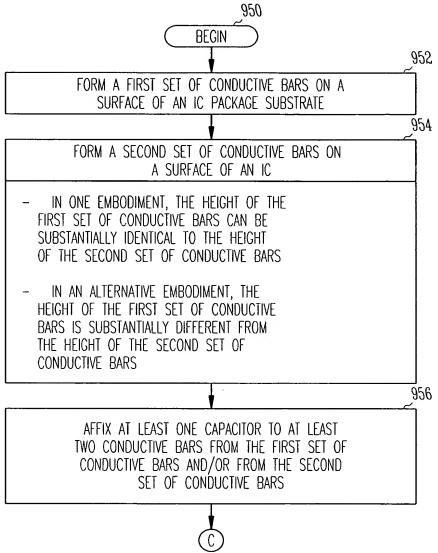


Fig.29A

TITLE: INTEGRATED CIRCUIT PACKAGES WITH SANDWICHED CAPACITORS (AS AMENDED)

INVENTOR NAME: Priyavadan R. Patel et al. SERIAL NO.: 10/006,292

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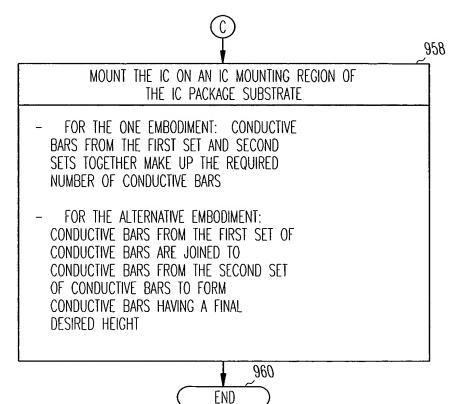


Fig.29B